REMARKS

Claims 1-12 are pending in the present application. Claim 4 has been amended to enhance readability. Claims 1 and 8 are independent.

Initially, Applicants appreciate the Examiner's recognition of claims 4 and 5 as allowable subject matter. As to the reasons for allowance, Applicants assert that references to Fig. 10, element 70, PVT MAX and PVTMIN by the Examiner are exemplary embodiments and not necessarily the only possible embodiments of claims 4 and 5.

With regard to the Examiner's objection to the specification, Applicants assert that the objection is now moot given the amendment to the specification as per the Examiner's guidance.

With regard to the Examiner's objection to the drawings regarding the lack of "Prior Art" designation of Figs. 1-4, Applicants assert that the drawings have been amended to reflect that they are prior art. A Drawing Change Authorization Request is filed concurrently herewith. Applicants respectfully request that the objection to the drawings be withdrawn.

With regard to the Examiner's objection to the drawings based on 37 C.F.R. §1.84(p)(5), Applicants assert that the specification is compliant with 37 C.F.R. 1.85(p)(5). 37 C.F.R. §1.85(p)(5) generally states that reference characters mentioned in the description must appear in the drawings. The Examiner has objected to the use of the language "DELC1V15" in the specification description referring to drawings where the term "DELC1V15" is not shown in the drawings. Applicants point out that on page 3,

paragraph 9, the term "DELC1V15" is introduced as an exemplary type of small delay cell SDn where the small delay cells SDn are annotated, *inter alia*, in Fig. 2. Reference characters SDn in the specification description appear in the drawings, *inter alia*, Fig. 2 in compliance with 37 C.F.R. §1.85(p)(5). Since a DELC1V15 delay component is an exemplary type of small delay SDn, and SDn components are disclosed in, *inter alia*, Fig. 2, it is not necessary to include "DELC1V15" language in Fig. 2.

With regard to the Examiner's objection to claim 4, Applicants assert that the objection is now moot given the amendment to claim 4 as per the Examiner's guidance.

Rejections Under 35 U.S.C. §112

Claims 1-7 are rejected under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. Applicants respectfully traverse.

Applicants assert that claim 1 recites essential elements of an aspect of the invention, particularly the language regarding a "second pulse signal". The inclusion of elements into the claims that may contribute to a second pulse signal such as those suggested by the Examiner: a three-bit counter 51, decoder 52, and modules 53 and 54 would limit the claims beyond that which is required by MPEP §2172.01and may cause Applicants to incur lesser protections for their invention than the protections they are allowed under current patent law. For at least this reason, Applicants respectfully request that the 35 U.S.C. §112, second paragraph rejection of claims 1-7 be withdrawn.

Rejections Under 35 U.S.C. §102

Claims 1 and 2 are rejected under 35 U.S.C. §102(e) as being anticipated by Guinea et al. Applicants respectfully traverse.

With regard to claim 1, Applicants assert that Guinea et al. fail to disclose a plurality of sampling modules as recited in claim 1. Instead, Guinea et al. disclose one sampling module (Fig. 2, element 3).

Moreover, Guinea et al. fail to disclose a sampling module receiving a second pulse signal as recited in claim 1. Instead, Guinea et al. disclose in Fig. 2 the same pulse signal (CKin) used for both a delay circuit 1 and sample circuit 3.

Furthermore, Guinea et al. fail to disclose a sampling module being clocked by a tapped output signal as recited in claim 1. Instead, Guinea et al. disclose at Fig. 2 and Col. 3, lines 25-34 a sampling module 3 being synched by a periodic input signal (CKin) and with tapped signals (CK1-CKN) as inputs to the sampling module 3. Sampling module 3 outputs a word 4 representing CK1-CKN having N bits. The tapped output signals (CK1-CKN) of Guinea et al. are not used to clock a sample circuit as recited in claim 1.

Moreover, Guinea et al. fail to disclose a sampling module being clocked by a tapped output signal from one of a plurality of tapped delay cells as recited in claim 1. Instead, Guinea et al. disclose in Fig. 2 one sampling circuit using inputs from a plurality of tapped delay cells.

Furthermore, Guinea et al. fail to disclose, as asserted by the Examiner, an encoder as recited in claim 1. Instead, Guinea et al. disclose at Figs. 2 and 9 and Col. 3, lines 34-37 a decoder 5 which includes AND gates A1-A15.

For at least these reasons, Applicants assert that Guinea et al. do not disclose each and every element of independent claim 1 and respectfully request that the 35 U.S.C. §102(e) rejection of claim 1 be withdrawn and that independent claim 1 be allowed.

With regard to claim 2, Applicants assert that it is not inherent that the system of Guinea et al. produces an output value that represents process, voltage, and temperature (PVT) conditions of a microchip as recited in claim 2. Instead, Applicants assert that Guinea et al. accurately discloses in Fig. 2 and Col. 3, lines 37-42 an output 6 of a circuit 2 being control information. For at least this reason, Applicants assert that it is not inherent that output 6 represent PVT conditions of a microchip as disclosed by Guinea et al.

Furthermore, with regard to claim 2, Applicants assert that it is allowable for its own merits and because it depends from independent claim 1 which the Applicants believe has been shown to be allowable.

Claims 8 and 9 are rejected under 35 U.S.C. §102(b) as being anticipated by Kondoh et al. Applicants respectfully traverse.

With regard to claim 8, Applicants assert that Kondoh et al. fail to disclose a delay compensation circuit for measuring the process, voltage, and temperature (PVT) conditions of a microchip and outputting a value representative of said measured PVT conditions as recited in claim 8. Instead, Kondoh et al. is silent as to the measurement of

PVT and an output representing PVT conditions, and PVT related output being used as a control signal as recited in claim 8.

Furthermore, the system of Kondoh et al. fail to disclose an output value representative of measured PVT conditions used to generate a control signal for a variable delay component. Instead, Kondoh et al. disclose at Fig. 43 and Col. 17, lines 15-24 and Col. 37, lines 6-9 a control output 157 being a function of a phase comparator 15, charging pump circuit 16, loop filter 17, and an analog to digital converter 45. Applicants assert that Kondoh et al. fail to disclose the output 157 of elements 15, 16, 17, and 45 representing PVT conditions.

For at least these reasons, Applicants assert that Kondoh et al. do not disclose each and every element of independent claim 8 and respectfully request that the 35 U.S.C. §102(e) rejection of claim 8 be withdrawn and that independent claim 8 be allowed.

With regard to claim 9, Applicants assert it is allowable for its own merits and because it depends from independent claim 8 which the Applicants believe has been shown to be allowable.

Rejections Under 35 U.S.C. §103

Claims 3 and 7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Guinea et al. in view of Lee et al. Applicants respectfully traverse.

With regard to claims 3 and 7, Applicants assert that they are allowable for their own merits and because they depend from independent claim 1 which the Applicants believe has been shown to be allowable.

Claims 6 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Guinea et al. in view of Fig. 2 of the present application. Applicants respectfully traverse.

With regard to claims 6 and 10, Applicants assert they are allowable for their own merits and because they depend from one of independent claims 1 and 8 which the Applicants believe have been shown to be allowable.

Claim 11 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kondoh et al. in view of Guinea et al. Applicants respectfully traverse.

With regard to claim 11, Applicants assert it is allowable for its own merits and because it depends from independent claim 8 which the Applicants believe has been shown to be allowable.

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kondoh et al. in view of Guinea et al. as applied to claim 11, and further in view of Lee et al. Applicants respectfully traverse.

With regard to claim 12, Applicants assert it is allowable for its own merits and because it depends from independent claim 8 which the Applicants believe have been shown to be allowable.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-12 are patentable over the relied upon references, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

Pursuant to 37 C.F.R. §§1.17 and 1.136(a), the Applicants respectfully petition for a one (1) month extension of time for filing a response in connection with the present application, and the required fee of $110.00 is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment of Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. §1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C.

By _____

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JAC/RFS:ewd

Attachment: Marked-up Version
Drawing Change Authorization Request

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The specification has been amended as follows:

On page 4, please replace paragraph [0015] containing lines 19-21 with the following rewritten paragraph:

--The variable delay control circuit 100 of Fig. [2] 3 can be considered a type of delay-locked loop (DLL), because it synchronizes or aligns the delayed clock signal P_CK with the input clock signal CLK.--

IN THE CLAIMS

The claims have been amended as follows:

4. (Amended) The apparatus of claim 1, further comprising:

a variation circuit for receiving said generated output value [generated] and comparing said generated output value to a previously stored maximum output value and a previously stored minimum output value,

wherein, if said generated output value is less than said previously stored minimum output value, said generated output value is stored as said minimum output value, and

wherein if said generated output value is greater than said maximum output value, said generated output value is stored as said maximum output value.